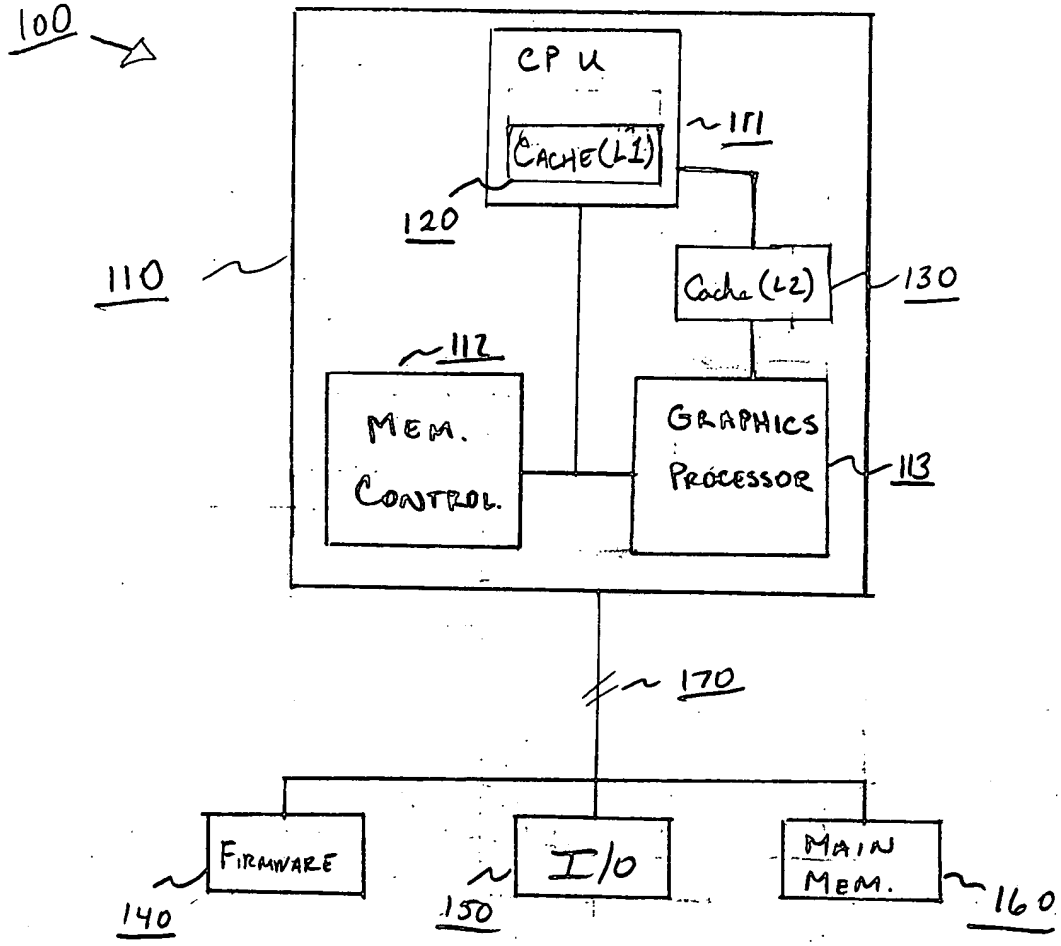

100
CPU
CACHE(L1)
111
120
110
Cache (L2)
130
112
MEM. CONTROL
GRAPHICS PROCESSOR
113
170
FIRMWARE
I/O
MAIN MEM.
140
150
160

FIG. 1

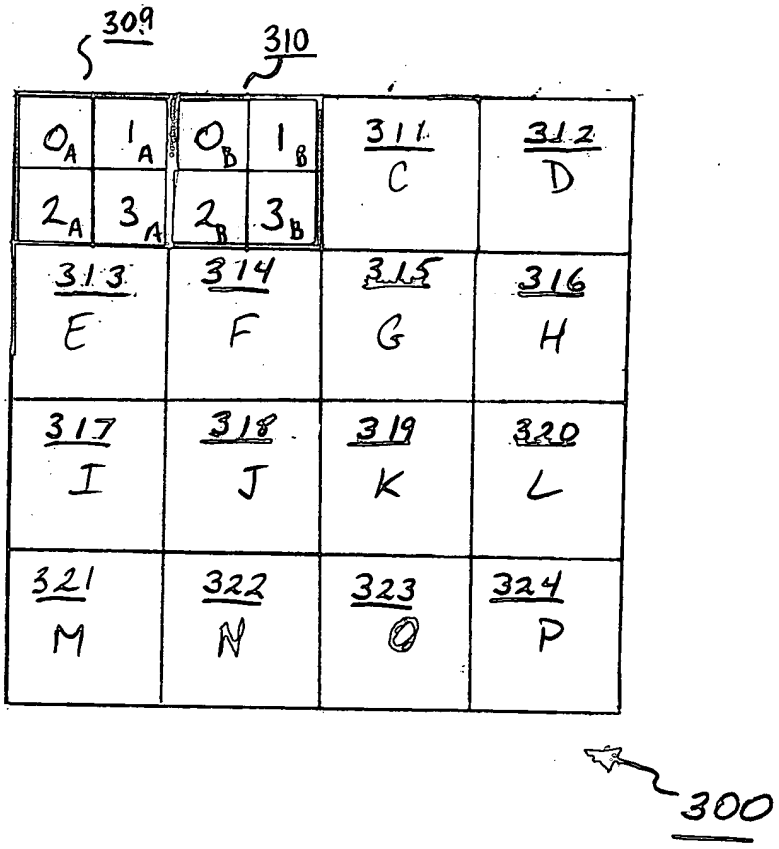
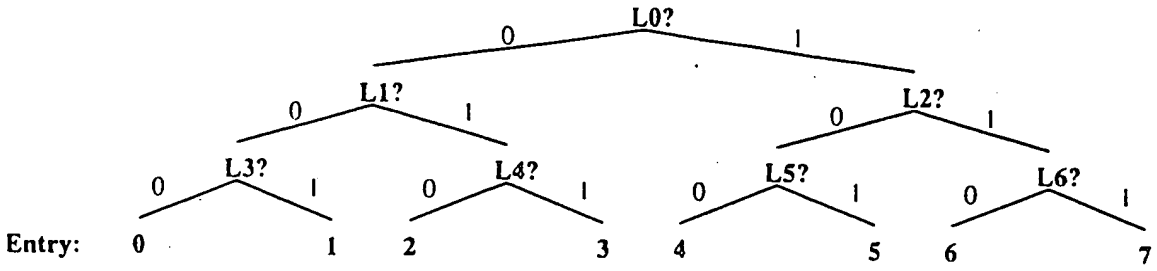

309
310
0_A 1_A 2_A 3_A
0_B 1_B 2_B 3_B
311
C
312
D
313
E
314
F
315
G
316
H
317
I
318
J
319
K
320
L
321
M
322
N
323
O
324
P
300

FIG. 2

PSEUDO-LRU REPLACEMENT MECHANISHM



PSEUDO-LRU UPDATE BASED ON ENTRY HIT

Entry hit	New LRU value						
	L0	L1	L2	L3	L4	L5	L6
0	1	1		1			
1	1	1		0			
2	1	0			1		
3	1	0			0		
4	0		1			1	
5	0		1			0	
6	0		0				1
7	0		0				0

FIG. 3

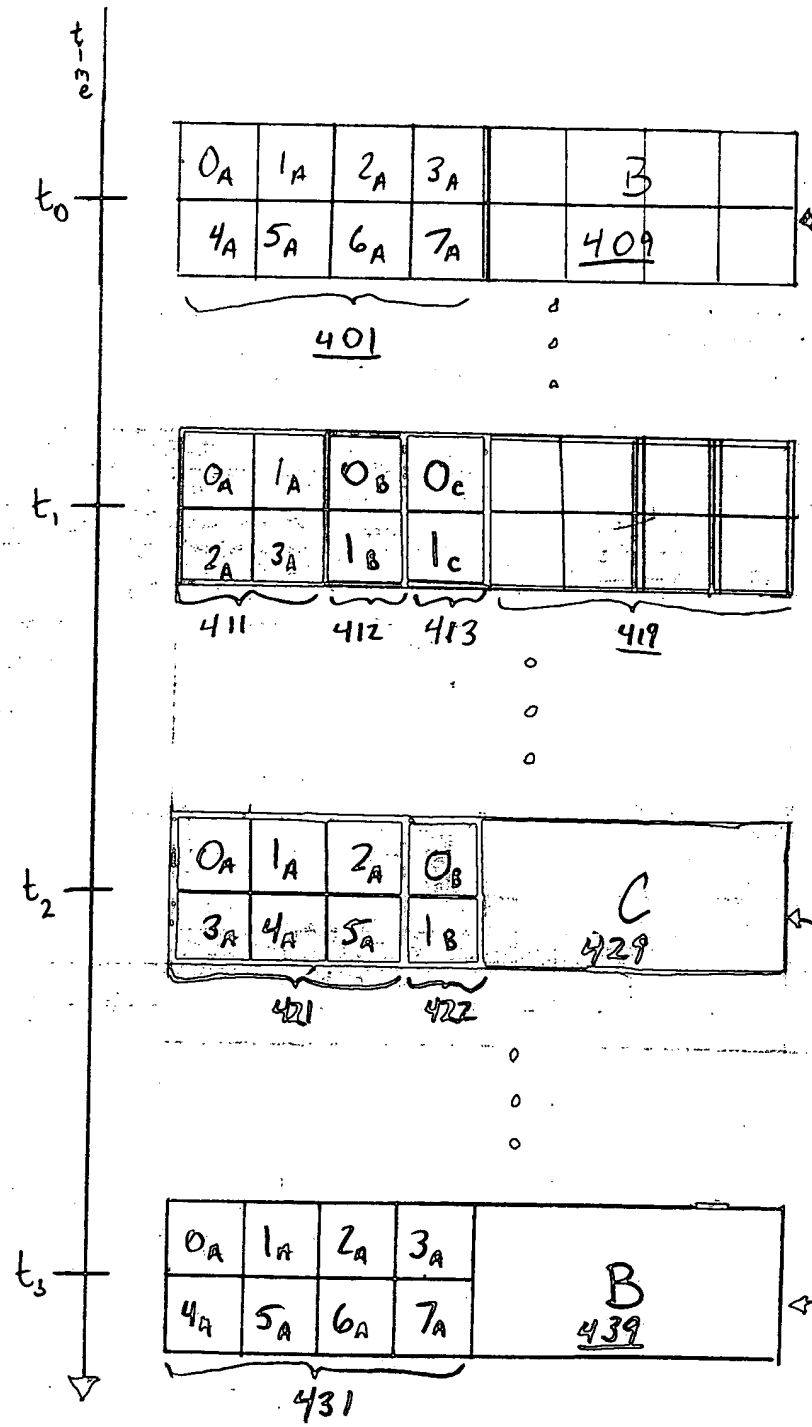


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D

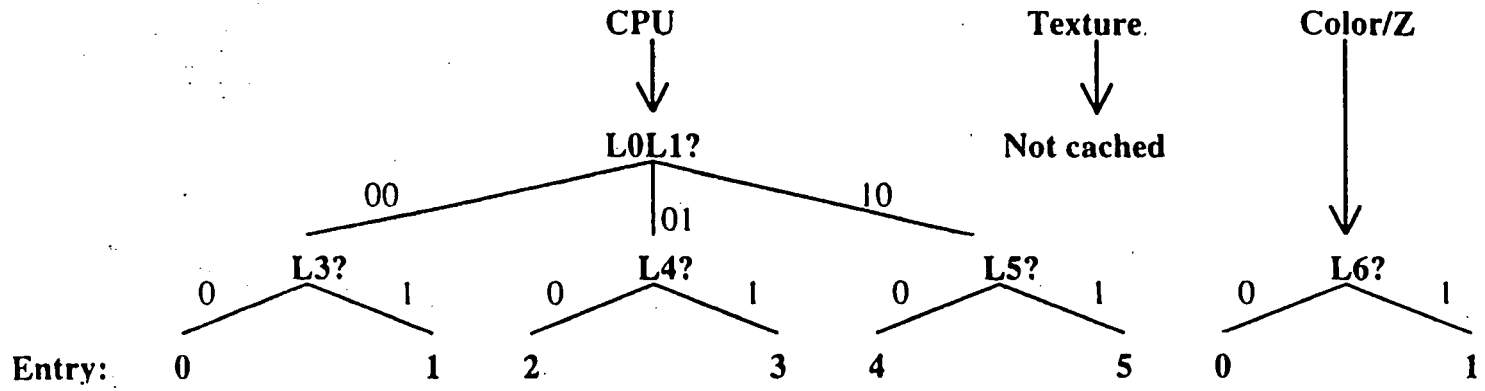

CPU
Texture
Color/Z
L0L1?
Not cached
00
01
10
L3?
L4?
L5?
L6?
0
1
0
1
0
1
0
1
Entry:
0
1
2
3
4
5
0
1

FIG. 5

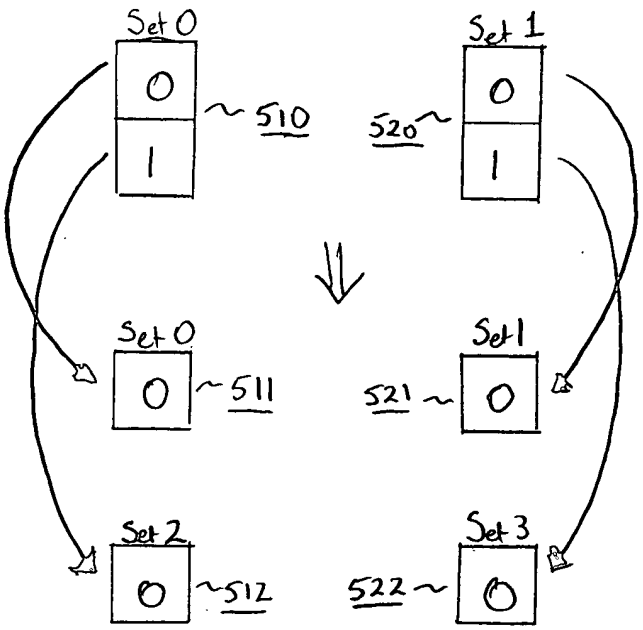
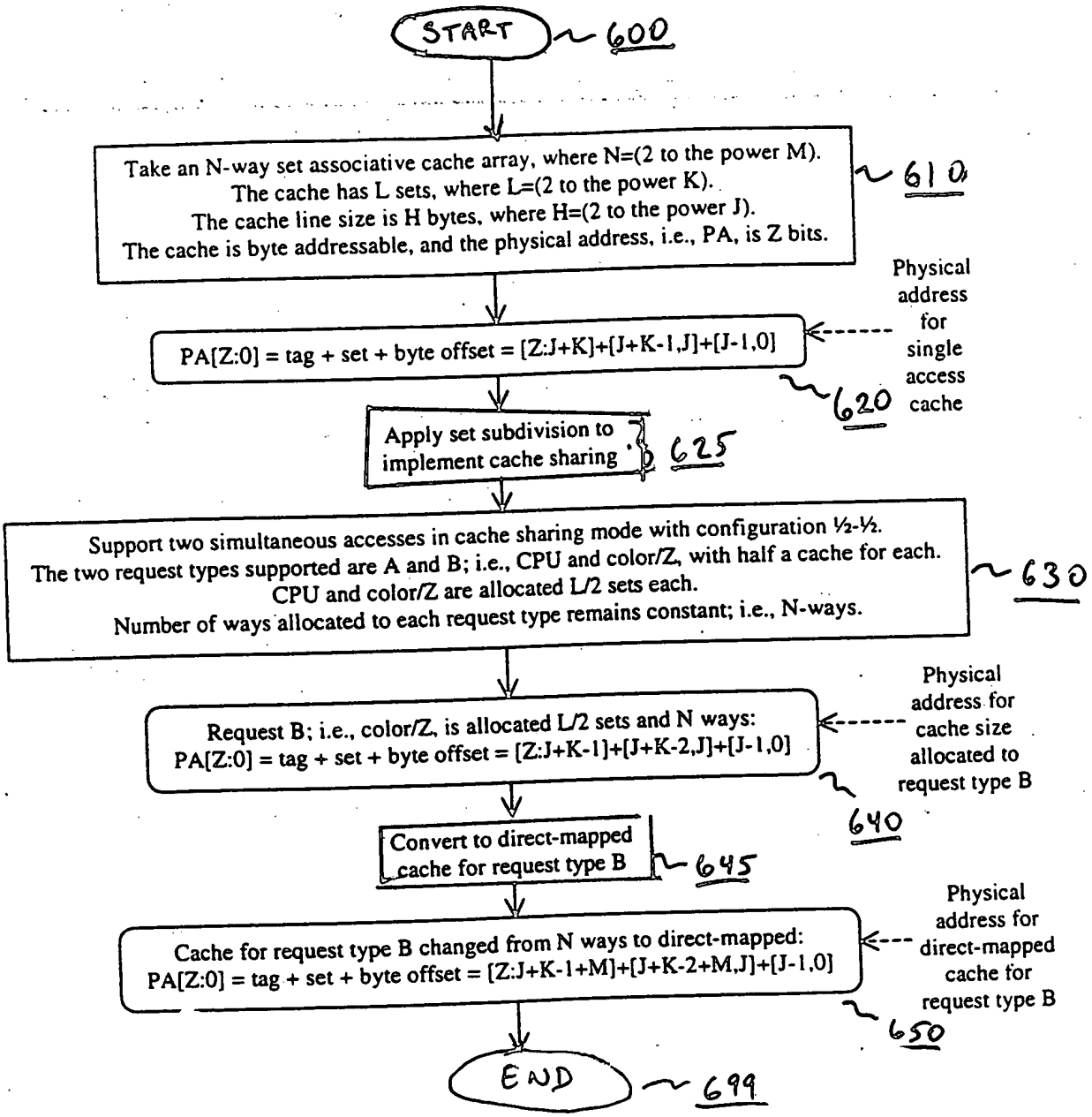
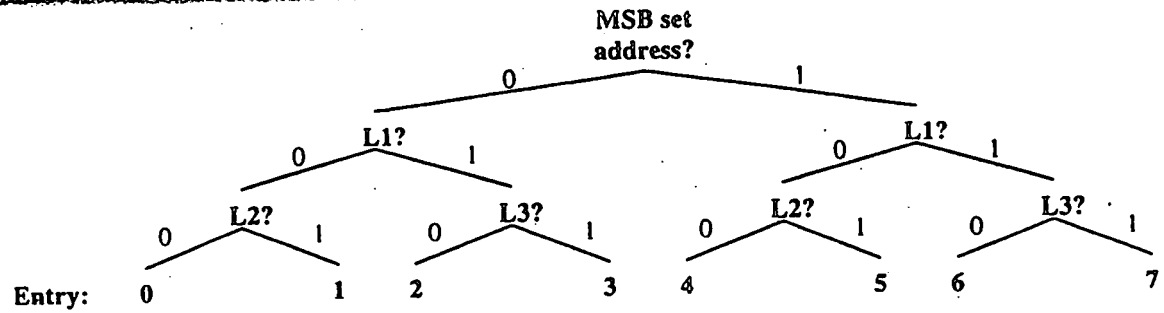

Set 0
0
1
510
Set 1
520
0
1
Set 0
0
511
Set 1
521
0
Set 2
0
512
Set 3
522
0

FIG. 6

500

FIG. 7


START
600
Take an N-way set associative cache array, where N=(2 to the power M).
The cache has L sets, where L=(2 to the power K).
The cache line size is H bytes, where H=(2 to the power J).
The cache is byte addressable, and the physical address, i.e., PA, is Z bits.
610
PA[Z:0] = tag + set + byte offset = [Z:J+K]+[J+K-1,J]+[J-1,0]
Physical address for single access cache
620
Apply set subdivision to implement cache sharing
625
Support two simultaneous accesses in cache sharing mode with configuration ½-½.
The two request types supported are A and B; i.e., CPU and color/Z, with half a cache for each.
CPU and color/Z are allocated L/2 sets each.
Number of ways allocated to each request type remains constant; i.e., N-ways.
630
Request B; i.e., color/Z, is allocated L/2 sets and N ways:
PA[Z:0] = tag + set + byte offset = [Z:J+K-1]+[J+K-2,J]+[J-1,0]
Physical address for cache size allocated to request type B
640
Convert to direct-mapped cache for request type B
645
Cache for request type B changed from N ways to direct-mapped:
PA[Z:0] = tag + set + byte offset = [Z:J+K-1+M]+[J+K-2+M,J]+[J-1,0]
Physical address for direct-mapped cache for request type B
650
END
699



PSEUDO-LRU UPDATE BASED ON ENTRY HIT

Entry hit	New LRU value			
	MSB	L1	L2	L3
0	1	1	1	
1	1	1	0	
2	1	0		1
3	1	0		0
4	0	1	1	
5	0	1	0	
6	0	0		1
7	0	0		0

FIG. 8